AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) A clock signal detection circuit, comprising:

a first circuit generating an output signal of predetermined potential in accordance with a first level of a clock signal, and setting an output terminal to a high impedance state in accordance with a second level of the clock signal;

an impedance element that is disposed between the output terminal of the first circuit and a potential source having a potential that is different from the predetermined potential, and that maintains the output signal above a first threshold when the output terminal is in the high impedance state for less than a first period; and

a second circuit generating a clock signal detection result ~~in accordance with an output potential of the first circuit~~ that is a first state when the output signal is above the first threshold and is a second state when the output signal is below the first threshold,

wherein the output signal decreases below the first threshold when the output terminal is in the high impedance state for greater than or equal to the first period.

2. (Original) A clock signal detection circuit, comprising:

a first circuit generating a first output signal of predetermined potential in accordance with a first level of a clock signal, and setting an output terminal of the first circuit to a high impedance state in accordance with a second level of the clock signal;

a first impedance element disposed between the output terminal of the first circuit and a first potential source having a potential that is different from the predetermined potential;

a second circuit generating a second output signal in accordance with an output potential of the first circuit;

a third circuit generating a third output signal with the predetermined potential in accordance with the second level of the clock signal, and setting an output terminal of the third circuit to the high impedance state in accordance with the first level of the clock signal;

a second impedance element disposed between the output terminal of the third circuit and a second potential source having a potential that is different from the predetermined potential;

a fourth circuit generating a fourth output signal in accordance with an output potential of the third circuit; and

a fifth circuit generating a clock signal detection result based on output signals of the second and the fourth circuit.

3. (Original) A clock signal detection circuit according to claim 1, wherein the impedance element includes one of a resistor and a transistor.

4. (Original) A clock signal detection circuit according to claim 2, wherein at least one of the first and second impedance elements includes one of a resistor and a transistor.

5. (Currently Amended) A semiconductor integrated circuit, comprising:

a first circuit generating an output signal of a predetermined potential in accordance with a first level of a clock signal, and setting an output terminal to a high impedance state in accordance with a second level of the clock signal; and

a second circuit generating a clock signal detection result that is a first state when the clock signal is at the first level and when the clock signal is at the second level for less than a first period, and that is a second state when the clock signal is at the second level for greater than or equal to the first period, wherein ~~in accordance with an output potential of the first circuit with~~ an impedance element disposed between the output terminal of the first circuit and a potential source having a potential that is different from the predetermined potential determines the first period.

6. (Original) A semiconductor integrated circuit, comprising:

a first circuit generating a first output signal of a predetermined potential in accordance with a first level of a clock signal, and setting an output terminal of the first circuit to a high impedance state in accordance with a second level of the clock signal;

a second circuit for generating a second output signal in accordance with an output potential of the first circuit with a first impedance element disposed between the output terminal of the first circuit and a first potential source having a potential that is different from the predetermined potential;

a third circuit generating a third output signal of the predetermined potential in accordance with a second level of the clock signal, and setting an output terminal of the third circuit to the high impedance state in accordance with the first level of the clock signal;

a fourth circuit generating a fourth output signal in accordance with an output potential of the third circuit with a second impedance element disposed between the output terminal of the third circuit and a second potential source having a potential that is different from the predetermined potential; and

a fifth circuit generating a clock signal detection result based on output signals of the second and the fourth circuit.

7. (Original) A semiconductor integrated circuit according to claim 5, wherein the impedance element includes one of:

an external resistor; and

a resistor and a transistor formed inside the semiconductor integrated circuit.

8. (Original) A semiconductor integrated circuit according to claim 6, wherein at least one of the first and second impedance elements includes one of:

an external resistor; and

a resistor and a transistor formed inside the semiconductor integrated circuit.